Status of the Claims

The listing of claims will replace all prior versions, and listings of claims in the application.

1. (Original) A method for transition delay matching comprising:

receiving a divided clock signal at a divided clock signal input section from a clock signal divider device;

producing an output signal in a clock buffer section based on an input signal from the divided clock signal input section; and

limits the amplitude of the output signal using an amplitude adjusting section, wherein the limiting of the amplitude of the output signal reduces a time for the output signal to reach a steady state value.

2. (Original) The method of claim 1, wherein:

receiving a plurality of the clock signals from the clock signal divider device, wherein first and second clock signals of the plurality of the clock signals are 180° out of phase with respect to each other;

producing first and second output signals in the clock buffer section based on the first and second clock signals; and

limiting a divided clock steady state voltage differential between the amplitudes of the first and second clock signals using the amplitude adjusting section.

3. (Original) The method of claim 2, further comprising positioning a resistor between first and second respective output nodes of the clock buffer section.

4. (Currently Amended) The ~~system~~ method of claim 2, further comprising:

coupling a voltage source to a common node in the amplitude adjusting section;

coupling a first resistor between a first output node of the clock buffer section and the common node and using the first resistor to generate the first one of the output signals; and

coupling a second resistor between a second output node of the clock buffer section and the common node and using the second resistor to generate the second one of the output signals.

5. (Original) The method of claim 1, wherein:

receiving first and second clock signals at the divided clock signal input section that are 180° out of phase with respect to of each other;

producing first and second output signals using the clock buffer section based on the first and second clock signals; and

limiting a divided clock steady state voltage differential between the first one of the output signals and the second one of the output signals using the amplitude adjusting section.

6. (Currently Amended) The method of claim 5, further comprising coupling a ~~resister~~ resistor between first and second output nodes on the clock buffer section that output the first and second output signals.

7. (Original) The method of claim 5, further comprising:

coupling a voltage source to a common node in the amplitude adjusting section;

coupled a first resistor between a first output node of the clock buffer section and the common node; and

coupling a second resistor between a second output node of the clock buffer section and the common node.

8. (Original) The method of claim 1, further comprising:

receiving first and second clock signals 180° out of phase with respect to each other at the divided clock signal input section;

producing a first one of the output signals based on the first clock signal using a first clock buffer device in the clock buffer section;

producing a second one of the output signals using a second clock buffer device in the clock buffer section based on the second clock signal; and

limiting a divided clock steady state voltage differential between the first one of the output signals and the second one of the output signals using the amplitude adjusting section.

9. (Original) The method of claim 8, further comprising:

coupling a first resistor between an output terminal on the first output buffer device that outputs the first one of the output signals and a voltage source; and

coupling a second resistor between an output terminal on the second output buffer device that outputs the first one of the output signals and a voltage source.

10. (Original) The method of claim 1, further comprising coupling a resistor between the clock buffer section and a voltage supply in the amplitude adjusting section.

11. (Original) A method comprising:

generating first and second clock signals;

produces clock output signals at first and second clock signal output terminals based on the first and second clock signals;

dividing the first and second clock signals into first and second divided clock signals that are 180° out of phase with respect to each other; and

producing first and second divided clock output signals at first and second divided clock signal output terminals based on the first and second clock signals received at first and second input terminals, such that there is a reduction in time in a transition of the amplitude of the first and second divided clock output signals to a steady state value.

12. (Original) The method of claim 11, further comprising:

produces the first and second divided clock output signals using a clock buffer section; and

limiting the amplitude of the first and second divided output signals using an amplitude adjusting section.

13. (Currently Amended) The ~~system~~ method of claim 12, further comprising limiting a divided clock steady state voltage differential between the amplitudes of the first and second divided clock output signals using the amplitude adjusting section.

14. (Currently Amended) The ~~system~~ method of claim 12, further comprising coupling a resistor coupled between the first and second output terminals in the amplitude adjusting section.

15. (Original) The method of claim 12, further comprising:

coupling a voltage source to a common node in the amplitude adjusting section;

coupling a first resistor between the a first output terminal and the common node; and

coupling a second resistor between the second terminal and the common node.

16. (Original) The method of claim 12, further comprising:

coupling a first clock buffer device to the first input terminal that produces the first divided clock output signal in the clock buffer section; and

coupling a second clock buffer devices to the second input terminal that produces the second divided clock output signal in the clock buffer section;

limiting a divided clock steady state voltage differential between the first and second divided clock output signals using the amplitude adjusting section.

17. (Original) The method of claim 16, further comprising:
coupling a first resistor between an output terminal of the first output buffer device and a voltage source; and

coupling a second resistor between an output terminal of the second output buffer device and a voltage source.